CBCS SCHEME

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18CS33

Third Semester B.E. Degree Examination, June/July 2023
Analog and Digital Electronics

Time: 3 hrs. Max. Marks: 100

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. With neat diagram, explain construction, working principle and V-I characteristics of photodiode. **(10 Marks)**

b. Explain the operation of Astable Multivibrator using IC-555, also shows the circuit configuration, waveforms and relevant supporting voltage and time expressions. **(10 Marks)**

OR

2 a. Discuss the working of Relaxation Oscillator with neat supporting diagram. Derive the expression for total time required for one oscillation. **(10 Marks)**

b. Define the following terms with respect to voltage regulator:
(i) Load Regulation (ii) Line Regulation (iii) Voltage stability factors **(05 Marks)**

c. Explain the connection of LM317 adjustable voltage regulator. **(05 Marks)**

Module-2

3 a. Fig.Q3(a) shows for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition and the headlights respectively. Design the logic circuit with these switches as input so that the alarm will be activated wherever either of the following conditions exists.
(i) The headlights are on while the ignition is off.
(ii) The door is open while the ignition is on.
Write truth table and use K-map to get simplified expression implement the same using basic gates.

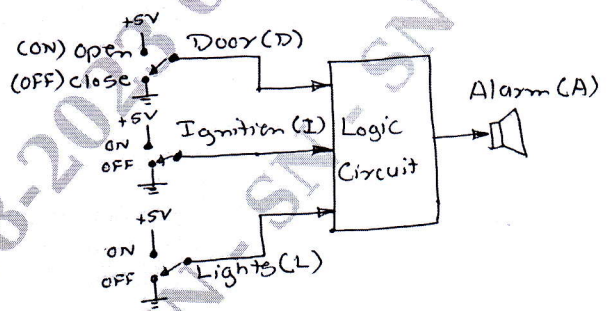

Fig.Q3(a) **(10 Marks)**

b. Find the minimum sum of product using K-map for each function.
(i) $f(a, b, c, d) = \pi M(0, 1, 6, 8, 11, 12).\pi D(3, 7, 14, 15)$
(ii) $f(a, b, c, d) = \sum m(1, 3, 4, 11) + \sum d(2, 7, 8, 12, 14, 15)$ **(10 Marks)**

OR

4 a. For the following function, find a minimum sum of product solution using the Quine-McCluskey method: $f(a, b, c, d) = \sum m(1, 3, 4, 5, 6, 7, 10, 12, 13 + \sum d(2, 9, 15)$ **(08 Marks)**

b. Find all prime implicants of the following function and then find all minimum solutions using Petrick's method:
$F(A, B, C, D) = \sum m(9, 12, 13, 15) + \sum d(1, 4, 5, 7, 8, 11, 14)$ **(12 Marks)**

Module-3

5 a. Define static hazards. With neat supporting circuit, K-map and Timing diagram, explain Static-1 Hazard. Also explain how static - 1 hazard can be removed from circuit. **(12 Marks)**

b. (i) Show how two 2-to-1 MUX (with no added gates) could be connected to form 3 to 1 MUX. Input selection should be as follows:
If AB = 00, select I_0
If AB = 01, select I_1
If AB = 1X (B is a don't care) select I_2

(ii) Show how two 4 to 1 and one 2 to 1 MUX could be connected to form an 8 to 1 MUX with three control inputs.

(iii) Show how four 2 to 1 and one 4 to 1 MUX could be connected to form an 8 to 1 MUX with three control inputs. **(08 Marks)**

OR

6 a. For each item, indicate whether it is referring to a decoder, an encoder or a MUX.
(i) Has more input than outputs.
(ii) Produces a binary code at its output.
(iii) Only one of its outputs can be active at one time.
(iv) Uses SELECT inputs.
(v) Can be used to generate arbitrary logic functions **(05 Marks)**

b. Realize a full adder using a 3 to 8 line decoder and (i) two OR gates (ii) two NOR gates. **(05 Marks)**

c. With neat supporting diagram compare PLA and PAL. Implement the following equation using PLA:
$X = AB'D + A'C' + BC + C'D'$
$Y = A'C' + AC + C'D'$
$Z = CD + A'C' + AB'D$ **(10 Marks)**

Module-4

7 a. Write a VHDL module that implements a half adder, a full adder, a half substractor and a full substractor. **(10 Marks)**

b. Write a VHDL module for 8 to 1 MUX. **(05 Marks)**

c. Draw the circuit represented by the following VHDL statements.
F < = E and I;
I < = G or H;
G < = A and B;
H < = not C and D; **(05 Marks)**

OR

8 a. Explain the working of SR Latch with neat circuit diagram, truth table and timing diagram. **(10 Marks)**

b. With a neat logic diagram, truth table and timing diagram, explain the working of J-K Master Slave flip-flop. **(10 Marks)**

Module-5

9 a. Discuss the working of n-bit parallel adder with accumulator. **(10 Marks)**

b. Implement the shift register using MUX and D flip-flop and write the timing diagram for the same. **(10 Marks)**

OR

10 a. Design a 3-bit synchronous binary counter using T-flip flop. Write transition table, K-map and circuit diagram. **(08 Marks)**

b. Design a 3-bit counter which counts in the sequence:
001, 011, 010, 110, 111, 101, 100, (Repeat) 001, ...
Use J-K flip-flop **(12 Marks)**